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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/622,780	07/21/2003	Atsushi Yusa	OKI.553	4253

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EXAMINER	
LE, DIEU MINH T	

ART UNIT	PAPER NUMBER
2114	

DATE MAILED: 04/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/622,780	YUSA, ATSUSHI	
	Examiner	Art Unit	
	Dieu-Minh Le	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/30&11/04/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is response to the communication filed on 12/30/03 in application 10/622,780.

2. Claims 1-16 are presented for examination.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-4, 6, 8-12, 14-15 are rejected under 35 U.S.C. 102(b) as being anticipated over Tuda et al. (U.S. Patent No. 5,132,937 hereafter referred to as Tuda).

As per claim 1:

Tuda explicitly teach the invention. Tuda teaches:

- A circuit for detecting an abnormal operation of memory [abstract, fig. 6, col. 2, lines 44-60] comprising:

- a delay circuit for delaying an output data of the memory for a predetermined period of time and for outputting this data as a delay data [fig. 6, col. 4, lines 2-41];

- a comparison circuit for outputting an incoincidence signal in case that the output data of the memory and the delay data are not coincident with each other after compared [fig. 6, col. 2, lines 44-60].

As per claim 2:

Tuda further explicitly teach:

- an access speed of memory is detected (i.e., ***read/write and storing to and from memory***) [fig. 6, col. 4, line 45 through col. 5, line 25].

As per claim 3:

Tuda further explicitly teach:

- a circuit for holding address information in case of an incoincidence in response to the incoincidence signal [fig. 6, col. 4, lines 2-41].

As per claim 4:

Tuda further explicitly teach:

- a circuit for sounding an alarm in outputting the incoincidence signal (i.e., ***indicating signal***) [fig. 6, col. 1, lines 57-67].

As per claim 6:

Tuda further explicitly teach:

- a delay time of the output data of the memory can be adjusted in the delay circuit [fig. 6, col. 4, lines 2-41 and col. 5, line 67 through col. 6, line 3].

As per claim 8:

Tuda further explicitly teach:

- an integrated circuit comprising a circuit for detecting an abnormal operation of memory (i.e., ***semiconductor memory device***) [abstract, fig. 6, col. 2, lines 44-60].

This is clearly shown that ***Tuda' semiconductor memory testing including a delay circuit, a comparison circuit, and input/output data*** capabilities do teach to Applicant's invention, more specifically to "a memory abnormal or error/failure operation" limitation.

As per claims 9-12, 14-15:

Due to the similarity of claims 9-12, 14-15 to claims 1-4, 6, 8 except for a method for detecting an abnormal operation of memory comprising delaying and output step, outputting an incoincidence signal step, comparison step, etc… instead of a circuit for detecting an abnormal operation of memory comprising capabilities of delaying, output, outputting an incoincidence signal, comparison, etc…; therefore, these claims are also rejected under the same rationale applied against claims 1-4, 6, 8. **In addition, all of the limitations have been noted in the rejection as per claims** 1-4, 6, 8.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 5, 7, 13, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tuda et al. (U.S. Patent No. 5,132,937 hereafter referred to as Tuda).

As per claims 5 and 7:

Tuda explicitly teach the invention. Tuda teaches:

- A circuit for detecting an abnormal operation of memory [abstract, fig. 6, col. 2, lines 44-60] comprising:
- a delay circuit for delaying an output data of the memory for a predetermined period of time and for outputting this data as a delay data [fig. 6, col. 4, lines 2-41].

Tuda does not explicitly teach:

- a circuit for executing an interruption;
- a flash memory.

However, Tuda does disclose capability of:

- a semiconductor memory testing including a delay circuit, a comparison circuit, and input/output data [abstract, fig. 6, col. 2, lines 44-60] comprising capabilities of:
- ***signal resetting and executing in supporting the memory failure detecting [col. 4, lines 20-41 and col. 5, lines 57-66]***.

- a semiconductor memory (i.e., ***flash memory***) [fig. 6, col. 1, lines 8-11].

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to realize that the Tuda's ***signal resetting and execution in the semiconductor memory*** capability does perform such Applicant's interrupting and flash memory limitations. This is because Tuda clearly applied these features therein for testing configuration, comparison, simulation, evaluation, performance in determining whether the memory system functioned properly. It is further obvious because these interrupting and flash memory features are notoriously well-known in the art of memory testing and failure/abnormal detection and correction arena. By applying the Tuda's ***signal resetting and execution in the semiconductor memory*** capability, the computer memory data processing system, more specifically an memory abnormal operation detection system can enhance its operation performance, more specifically to ensuring the error thoroughly detected and corrected via the delaying and comparison processes.

This modification would have been obvious because a person having ordinary skill in the art would have been motivated to do

so to improve the computer memory data system operation availability and network/system performance therein with a mechanism to enhance the data connectivity, data debugging, data displaying, data reliability, and data throughput which eventually will increase its performance, such as data throughput between internal and external devices.

As per claims 13 and 16:

Due to the similarity of claims 13 and 16 to claims 5 and 7 except for a method for detecting an abnormal operation of memory comprising delaying and output step, outputting an incoincidence signal step, comparison step, etc… instead of a circuit for detecting an abnormal operation of memory comprising capabilities of delaying, output, outputting an incoincidence signal, comparison, etc…; therefore, these claims are also rejected under the same rationale applied against claims 5 and 7. **In addition, all of the limitations have been noted in the rejection as per claims** 5 and 7.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kono et al. (U.S Patent 5,455,536) explicitly teaches a comparison circuit used for computer the data and its delay data for uncoincidence (i.e., error detection and correction process) [fig. 3, col. 2, line 51 through col. 4, line 23].

8. A shortened statutory period for response to this action is set to expired THREE (3) months, ZERO days from the date of this letter. Failure to respond within the period for response will cause the application to be abandoned. 35 U.S.C. 133.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dieu-Minh Le whose telephone number is (571) 272-3660. The examiner can normally be reached on Monday - Thursday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571)272-3644. The Tech Center 2100 phone number is (571) 272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DIEU-MINH THAI LE
PRIMARY EXAMINER
ART UNIT 2114

DML
03/30/06